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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/627,457 | 07/25/2003 | Andy T. Nguyen | X-1213 US | 3254 |

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| EXAMINER | |
|---|---|
| NGUYEN, HAI L | |
| **ART UNIT** | **PAPER NUMBER** |
| 2816 | |

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Offic Action Summary | Application N . | Applicant(s) | |
|---|---|---|---|
| | 10/627,457 | NGUYEN ET AL. | |
| | Examiner | Art Unit | |
| | Hai L. Nguyen | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --*

**Peri d for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *25 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,8,9,15,19 and 21-24* is/are rejected.

7)☒ Claim(s) *3-7,10-14,16-18 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the details of "an N-to-M multiplexer comprising ... N control terminals coupled to the N output terminals of the first bi-directional shift register" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

## *Specification*

2. The disclosure is objected to because of the following informalities: page 15, line 20; "1102" should be changed to --1002-- as shown in Fig.12. Appropriate correction is required.

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the recited limitation "an N-to-M multiplexer comprising ... N control terminals coupled to the N output terminals of the first bi-directional shift register", in claim 21, is not supported either by the disclosure or the drawings. There is insufficient antecedent basis for this limitation in the claim.

## *Claim Rejections - 35 USC § 112*

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 21-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 21 is indefinite because of the limitation "an N-to-M multiplexer comprising N data input terminals coupled to the N data input terminals of the multiplexer circuit, N control terminals coupled to the N output terminals of the first bi-directional shift register" on lines 7-1. It is unclear because it cannot be determined what kind of structural cooperative relationships of those elements is being claimed here.

Claims 22-24 are rejected due to their dependencies on claim 21.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 2, 8, 9, 15, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Farwell (US 5,870,445).

With regard to claims 1 and 15, Farwell discloses in Figs.1-3 a delay lock loop (DLL) circuit coupled between output and input terminals of a clock network (a portion of 19), the DLL circuit, and a method of use thereof, comprising an input clock terminal; a feedback clock terminal coupled to the output terminal of the clock network (FCLK); a delay line (13) having an input terminal coupled to the input clock terminal and having a plurality of output terminals providing a plurality of intermediate clock signals (outputs of $I_{(1)}$-$I_{(N)}$); a control circuit (23, 25, and another portion of 19); and a bi-directional shift register (51) and clock multiplexer ($M_{(1)}$-$M_{(N)}$) having a plurality of data input terminals coupled to the output terminals of the delay line, wherein the bi-directional shift register comprises a token bit (left input to the shift register 51) shifted under control of the control circuit, and wherein the clock multiplexer selects one of the intermediate clock signals, as determined by a location of the token bit within the bi-directional shift register, to supply to the output terminal (output of $M_{(1)}$).

With regard to claim 2, the output terminal of the bi-directional shift register and clock multiplexer is coupled to a third input terminal of the control circuit (input terminal

of another portion of 19, control circuit, which provides ECLK signal to the bi-directional shift register and clock multiplexer).

Claims 8, 9, and 19 are similarly rejected, note the above discussion with regard to claims 1 and 2.

### *Allowable Subject Matter*

8. Claims 3-7, 10-14, 16-18, and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record does not disclose or suggest a delay lock loop (DLL) circuit, and a method of use thereof, as recited in claims 3 and 10; specifically the limitation directed to the control circuit (403 in instant Fig.10) comprises a shift clock generator circuit (1001) and a shift enable circuit (1002, 1003); the shift clock generator circuit provides a plurality of control signals (CKA, CKB, CKC, CKD) to a first subset of the control input terminals (Ci's in instant Fig.6) of the bi-directional shift register and clock multiplexer (402 in instant Fig.6); and the shift enable circuit provides a plurality of shift enable signals (SLA, SLB, SLC, SLD, SRA, SRB, SRC, SRD) to a second subset of the control input terminals of the bi-directional shift register and clock multiplexer.

The prior art of record does not disclose or suggest a delay lock loop (DLL) circuit, and a method of use thereof, as recited in claims 6 and 13; specifically the limitation directed to wherein the bi-directional shift register and clock multiplexer (402 in instant Fig.6) comprises a plurality of shift register circuits (702 in instant Fig.7, 802 in instant Fig.8) coupled together through a plurality of multiplexer circuits (701, 801), each

of the shift register circuits being bi-directional and storing an associated token bit, each succeeding one of the shift register circuits comprising a smaller number of memory elements and each succeeding one of the multiplexer circuits comprising a smaller number of multiplexers until a single one of the shifted intermediate clocks signals has been selected (SEL_CLK).

The prior art of record does not disclose or suggest a system for synchronizing a feedback clock signal from a clock network with an input clock signal, and a method of use thereof, as recited in claims 18 and 20; specifically the limitation directed to means (1002/1003 in instant Fig.12) for verifying that a selected one of the two directions is compatible with a position of the first token bit within the first shift register (MA_0 - MA_15 in instant Fig.6), which has a very specific function as disclosed in the specification (page 15, line 19 through page 15, line 27).

The prior art of record does not disclose or suggest a method of synchronizing a feedback clock signal from a clock network with an input clock signal, as recited in claim 16; specifically the limitation directed to the step of shifting a second token bit in either of the two directions within a second shift register (MB_0 - MB_7/ MC_0 - MC_3/ MD_0 - MB_1 in instant Fig.6), wherein selecting from among the intermediate clock signals the selected clock signal based on the location of the first token bit within the first shift register (MA_0 - MA_15) further comprises selecting from among the intermediate clock signals (CLK0-CLK15) the selected clock signal based on a location of the second token bit within the second shift register.

***Conclusion***

9. Regarding claims 21-24, the patentability thereof cannot be determined because of their indefiniteness.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. For example, Lai et al. (US 6,333,959) is cited as of interest because it discloses a cross feedback latch-type bi-directional shift register in a delay lock loop circuit.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

HLN
June 25, 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800